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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,478	03/31/2004	James Loran Ball	ALTRP134/A1466	6370
51501 7590 04/24/2009 WEAVER AUSTIN VILLENEUVE & SAMPSON LLP - ALTERA ATTN: ALTERA P.O. BOX 70250 OAKLAND, CA 94612-0250				
EXAMINER GEIB, BENJAMIN P				
ART UNIT		PAPER NUMBER		
2181				
MAIL DATE		DELIVERY MODE		
04/24/2009		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action
Before the Filing of an Appeal Brief

Application No.

10/815,478

Applicant(s)

BALL, JAMES LORAN

Examiner

BENJAMIN P. GEIB

Art Unit

2181

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 08 April 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: _____.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____.
13. ☐ Other: _____.

/Alfred W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

/Benjamin P Geib/
Examiner, Art Unit 2181

Continuation of 11, does NOT place the application in condition for allowance because:

Regarding Applicant's argument that "Intel does not disclose or suggest 'wherein substantially all multi-byte aligned branch instructions are operable to access the instructions at byte aligned addresses,'" the Examiner notes that the Applicant appears to be reading the limitation too narrowly. The JMP instruction of Intel is operable to access instructions within the range of the offset used. See Intel, Vol. 2, page 3-357 "JMP-Jump" instruction reference. These instructions include "the instructions at byte aligned addresses." That is, the JMP is not prevented from accessing instructions at byte aligned addresses, but accesses instructions without regard as to whether they are byte-aligned or not. Therefore, Intel has taught "wherein substantially all multi-byte aligned branch instructions are operable to access the instructions at byte aligned addresses" as recited in the claims.

Applicant argues that "Intel, alone or in combination with Killian, fails to teach or render obvious the claim 1 limitation of 'common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate field in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions.'" The Examiner disagrees with this statement and notes that the Killian has taught an Address Unit (AU) 17 that performs sign-extension of branch and non-branch instructions. See Killian; column 11, lines 40-50. This AU 17 is subcircuitry of the overall processor. Furthermore, As noted by the Applicant in the remarks, Killian has taught "[a] sign-extension circuit 78 [that] sign-extends the 16-bit offset to 32 bits before the offset is combined at the adder." See Killian; column 11, lines 40-50. While Fig. 3C shows two separate blocks labeled "SE," these blocks are actually one sign-extension circuit. The Examiner notes that the "SE" block in the top right of Fig. 3C is not labeled differently from the "SE" block in the top left of Fig. 3C, which would be the case if the two block were two separate circuits. Further, as shown in Fig. 3C, the two "SE" block perform the same function of sign-extending the 16-bit offset from the instruction (whether a branch or non-branch instruction) to 32-bits. Therefore, Killian has taught common subcircuitry to perform sign extensions for branch and non-branch instructions as recited in the claims.